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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,264	01/11/2002	Satoshi Inaba	P 284163 01F181	6258

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,264	INABA, SATOSHI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-11* is/are rejected.

7)☒ Claim(s) *7-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statements filed 03/09/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed 04/29/2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,4,5,6 and 11 stand rejected under 35 U.S.C. 102(b) as being anticipated by YAZAWA et al. (4,819,043).

Yazawa et al. discloses a semiconductor device comprising a semiconductor substrate having a surface; a gate electrode 3 formed over the surface of said semiconductor substrate with a gate dielectric film 2 interposed therebetween; a pair 4-5 of source 4 and drain 5 diffusion layers formed in said semiconductor substrate to oppose each other with a channel region 6-7 laterally residing therebetween at a location immediately beneath said gate electrode 3, said source 4 and drain 5 diffusion layers each having a low (n++) resistivity region and an extension region 17 being formed to extend from this low resistivity region toward said channel region 6-7 and being lower (n+) in impurity concentration and shallower in depth than said low (n++) resistivity region; a first impurity doped layer 7 of a first (p) conductivity type formed in

said channel region 6-7 between the source/drain 4-5 diffusion layers; a second impurity doped layer 6 of a second (n) conductivity type formed under said first impurity doped layer 7; and a third impurity doped layer 1 of the first (p) conductivity type formed under said second impurity doped layer 6, wherein said three impurity doped layers make up a multilayer lamination structure with two p-n junctions 9 and 10, one 9 between said first 7 and second 6 impurity doped layers and the other 10 between said second 6 and third 1 impurity doped layer, wherein said first impurity doped layer 7 is equal to or less in junction depth than the extension region 17 of each of said source/drain 4-5 diffusion layers, and wherein said second impurity doped layer 6 is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first 7 and third 1 impurity doped layers, wherein said second impurity doped layer 6 is selectively formed in a region just beneath, or immediately beneath said gate electrode 3, said source/drain 4-5 diffusion layers are formed so that a bottom surface of the low resistivity region resides within said undoped semiconductor layer whereas a bottom surface of the extension region 17 is in contact with said second impurity doped layer 6, and wherein said gate electrode 3 is formed of a poly-silicon film. Note figures 7 and 15 and column 5 lines 13-28, column 8 lines 55-68, and column 9 lines 1-9 of Yazawa et al.

The applicant's claims 4 and 6 do not distinguish over the Yazawa et al. reference regardless of the process used to form the first and second impurity doped layers,

because only the final product is relevant, not the recited process of forming said layers into an undoped semiconductor layer as has been epitaxially grown.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over YAZAWA et al. (4,819,043).

Yazawa et al. discloses a semiconductor device with all the limitations of claims 2 and 3 except that the first impurity layer (the layer in which the channel is formed) is either partially or fully depleted. Note figures 5 through 8c, column 2 lines 20-24, column 7 lines 16-67, and column 8 lines 1-37 of Yazawa et al. It is noted that if the first impurity region is neither partially nor fully depleted, no channel can form, and the device will not function. Although Yazawa et al.'s device does not teach the exact types of depletion as that claimed by Applicant, the depletion differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

B. Claims 9 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over YAZAWA et al. (4,819,043) in view of CHEEK et al. (6,162,694).

Yazawa et al. discloses a semiconductor device with all the limitations of claims 9 and 10 except that the gate electrode is formed of a metal film as contacted with the gate electrode film. Note figures 5 through 8c, column 2 lines 20-24, column 7 lines 16-67, and column 8 lines 1-37 of Yazawa et al.

However, Cheek et al. discloses a method for replacing polysilicon gate electrodes with metal gate electrodes. Note figure 1 of Cheek et al. Therefore, it would have been obvious to a person having skill in the art to replace the polysilicon gate electrodes of Yazawa et al.'s semiconductor device with the metal gate electrodes such as taught by

Cheek et al. in order to reduce the conductivity and increase the electric field of the gate electrodes to thus provide a faster and more compact semiconductor device.

Allowable Subject Matter

4. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 04/29/2004 have been fully considered but they are not persuasive.

It is argued, at page 1 of the remarks, that "Yazawa et al. disclose a MOSFET with reduced short channel effect, otherwise known as a 'buried channel device.' In such a device, a channel is formed deep inside the substrate, not immediately beneath the gate electrode." However, Applicants' understanding of Yazawa et al.'s device appears to be contrary to Yazawa et al.'s own explanation of the device. Note column 5 lines 20-23, where Yazawa et al. state: "Referring to FIG. 7, a gate insulating film 2 is formed on a P-type semiconductor substrate 1, and a gate electrode 3 is formed on the gate insulating film 3.... A P-type layer 7 opposite in conductivity type to the source and drain regions 4 and 5 is formed in a surface portion of a channel formation region

lying beneath the gate insulating film 2." Here the Examiner has added emphasis to the words "surface portion," and "channel formation region."

It is further argued, at page 1 of the remarks, that "In the device of Yazawa et al. a channel is formed in an N-type layer 6 (in the ON state of the MOSFET only), not in the P-type layer 7. (See column 2, lines 20-34 and the crosshatched region of figure 3b)." The Examiner respectfully replies that Applicant's attention is directed at the wrong disclosed embodiment of Yazawa et al. The device of figure 3b and column 2 lines 20-34 is simply not cited above, and in the rejection mailed 1/29/04. Rather, it is the device of figure 7 that is cited against applicants' claims.

It is argued, at page 2 of the remarks, that "The Office Action on page 3, line 1, alleges that Yazawa et al. disclose a channel region 6-7. However, the P-type layer 7 of Yazawa et al. is not a channel region." In reply, once again it must be pointed out that at column 5 line 23 Yazawa et al. state that the "P-type layer 7 opposite in conductivity type to the source and drain regions 4 and 5 is formed in a surface portion of a channel formation region." There appears to be no distinction between applicants' claimed "channel region" and the "channel formation region" disclosed by Yazawa et al. at column 5 line 23.

It is further argued, at page 1 of the remarks, that "The P-type layer 7 of Yazawa et al. is not a channel region as it is of opposite conductivity type to the source/drain layers 4 or 5 and no "diffusion layer" is formed therein, even in the ON state of the MOSFET." However, in response to applicant's argument that the references fail to

show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the P-type layer 7 be a channel region – the claims simply require it to be a "a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers" – and that a diffusion layer be formed in P-type layer 7 – the claims actually require "diffusion layers formed in said semiconductor substrate." Note that in Yazawa et al.'s figure 7, diffusion layers 4 and 5 in fact are formed in Yazawa et al.'s semiconductor substrate, meeting the only "diffusion layer" limitation actually found in the claims as written) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
07/04

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